M68MPB916X1UM/D

October 1998

M68MPB916X1

MCU PERSONALITY BOARD

USER'S MANUAL

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CONTENTS

CHAPTER 1 GENERAL INFORMATION

1.1 INTRODUCTION 1-1
1.2 SPECIFICATIONS 1-2
1.3 EQUIPMENT REQUIRED 1-2
1.4 CUSTOMER SUPPORT 1-3

CHAPTER 2 HARDWARE PREPARATION AND INSTALLATION

2.1 INTRODUCTION 2-1
2.2 HARDWARE PREPARATION 2-1
2.2.1 Clock Select Header (W1) 2-4
2.2.2 VDDA Select Header (W2) 2-5
2.2.3 Voltage Reference High Select Header (W3) 2-6
2.2.4 Voltage Reference Low Select Header (W4) 2-7
2.2.5 VSSA Insertion Point (E1) 2-7
2.3 ANALOG/DIGITAL CIRCUITS 2-8
2.4 MEVB CONFIGURATION 2-9
2.5 ACTIVE PROBE CONFIGURATION 2-11

CHAPTER 3 MEVB QUICK START GUIDE

3.1 INTRODUCTION 3-1
3.2 CONFIGURING THE MPFB 3-1
3.2.1 MPFB Memory Devices 3-1
3.2.2 MPFB Jumper Headers 3-2
3.3 MEVB INSTALLATION INSTRUCTIONS 3-3
3.3.1 Power Supply – MPFB Connection 3-4
3.3.2 Personal Computer – BDM Connection 3-5
3.4 SOFTWARE INSTALLATION 3-6

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CHAPTER 4 MEVB SUPPORT INFORMATION

4.1 INTRODUCTION..... 4-1
4.2 LOGIC ANALYZER CONNECTOR SIGNALS..... 4-1

CHAPTER 5 MAPI SUPPORT INFORMATION

5.1 INTRODUCTION..... 5-1
5.2 MAPI BUS CONNECTORS..... 5-1

CHAPTER 6 SCHEMATIC DIAGRAMS

6.1 INTRODUCTION..... 6-1

FIGURES

2-1. MPB Parts Location Diagram (top view)..... 2-2
2-2. A/D Signal Filtering..... 2-8
2-3. MPB – MPFB Interconnection (with serial interface)..... 2-10
2-4. Active Probe Interconnection (with Active Probe Box)..... 2-12
5-1. MAPI Interface Connector Layout..... 5-1
5-2. MAPI Interface Connector P1 Pin Assignments..... 5-2
5-3. MAPI Interface Connector P2 Pin Assignments..... 5-3
5-4. MAPI Interface Connector P3 Pin Assignments..... 5-4
5-5. MAPI Interface Connector P4 Pin Assignments..... 5-5

TABLES

1-1. MPB Specifications..... 1-2
2-1. Jumper Header Types..... 2-3
2-2. MPB Jumper Header Descriptions..... 2-3
3-1. MPFB Quick Start Jumper Header Configuration..... 3-2
4-1. Logic Analyzer Connector J7 Pin Assignments..... 4-2
4-2. Logic Analyzer Connector J8 Pin Assignments..... 4-2
4-3. Logic Analyzer Connector J9 Pin Assignments..... 4-3
4-4. Logic Analyzer Connector J10 Pin Assignments..... 4-3
4-5. Logic Analyzer Connector J11 Pin Assignments..... 4-4

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TABLES (CONTINUED)

4-6. Logic Analyzer Connector J12 Pin Assignments..... 4-4
4-7. Logic Analyzer Connector J13 Pin Assignments..... 4-6
4-8. Logic Analyzer Connector J14 Pin Assignments..... 4-8
4-9. Logic Analyzer Connector J15 Pin Assignments..... 4-8
4-10. Logic Analyzer Connector J16 Pin Assignments..... 4-9
4-11. Logic Analyzer Connector J17 Pin Assignments..... 4-9
4-12. Logic Analyzer Connector J18 Pin Assignments..... 4-10
4-13. Logic Analyzer Connector J19 Pin Assignments..... 4-10
4-14. Logic Analyzer Connector J20 Pin Assignments..... 4-11

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CHAPTER 1
GENERAL INFORMATION

1.1 INTRODUCTION

This manual provides general information, hardware preparation, installation instructions, a quick start guide, and support information for the M68MPB916X1 MCU Personality Board (MPB). The MPB is one component of Motorola's modular approach to MC68HC916X1 Microcontroller Unit-based product development. This modular approach lets you easily configure our development systems to fit your requirements.

The MPB may be used in either the MMDS1632 Motorola Modular Development System (MMDS) or the modular evaluation board (MEVB). The MEVB consists of the M68MPFB1632 Modular Platform Board (MPFB) and an MPB. Alternately, you may install the MPB directly in your target system if the target system includes a modular active probe interconnect (MAPI) interface. The MCU device on the MPB defines which MCU is emulated/evaluated by the MMDS or evaluated by the MEVB. Both systems are invaluable tools for designing, debugging, and evaluating MCU operation of the M68HC16 and M68300 MCU families. By providing the essential MCU timing and I/O circuitry, these systems simplify user evaluation of prototype hardware/software products.

The MPB product includes:

- M68MPB916X1 MCU Personality Board (MPB)
- Plastic overlay for use with the MEVB – pin outs for the logic analyzer connectors on the MPFB (specifically for the MC68HC916X1 MCU)
- Documentation (this manual)

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1.2 SPECIFICATIONS

Table 1-1 lists MPB specifications.

Table 1-1. MPB Specifications

Characteristic	Specifications
On-Board Clock	Case style: 14 or 8-pin hybrid crystal clock oscillator (frequency as required by MCU).
External Clock	32 KHz – 16.78 MHz (or maximum MCU allows).
MCU I/O ports	HCMOS compatible
Temperature Operating Storage	 0° to +40° C -40° to +85° C
Relative humidity	0 to 90% (non-condensing)
Power requirements	+5 Vdc ± 5% @ 500 mA (max.)
Dimensions Size Weight	 3.25 x 3.25 in. (82.6 x 82.6 mm) 2.9 oz. (82.2 grams)

1.3 EQUIPMENT REQUIRED

The external requirements for MPB operation are either an MPFB or MMDS system. For MMDS operation requirements, see the MMDS1632 Motorola Modular Development System User's Manual,MMDS1632UM/D. For operation requirements for the MEVB, see this manual and the M68MPFB1632 Modular Platform Board User's Manual,M68MPFB1632/D. To use the MPB in an MEVB you must also have background debug mode (BDM) software and hardware (purchased separately) that communicates via BDM interface.

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CHAPTER 2
HARDWARE PREPARATION AND INSTALLATION

2.1 INTRODUCTION

This chapter provides unpacking instructions, hardware preparation information, and installation instructions for the MPB.

When you unpack the MPB from its shipping carton, verify that all items are in good condition. Save packing material for storing and shipping the MPB.

NOTE

Should the MPB arrive damaged, save all packing material, and contact the carrier's agent.

2.2 HARDWARE PREPARATION

This portion of the manual explains how to prepare the MPB before use, as well as how to configure the MPB for system operation. This section also explains MPB installation in the MMDS and MEVB.

The MPB has been factory tested and is shipped with installed jumpers. A jumper installed on a jumper header provides a connection between two points in the MPB circuit. The MPB has two types of jumper headers: three-pin and two-pin with a cut-trace short. A cut-trace short has a copper trace between the feed-through holes (bottom or solder side of the MPB). Table 2-1 describes each type of jumper header.

The MPB has four jumper headers (for which Table 2-2 is a quick reference guide). You may re-configured these jumper headers to customize MPB functionality. The following paragraphs explain each jumper header function. There is also an insertion point (E1) for connecting an external ground. Figure 2-1 shows the location of the MPB jumper headers and the insertion point.

NOTE

Verify that all socketed parts are seated in their sockets.

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CAUTION

Depending on your application, it may be necessary to cut the W2 wiring trace short (cut-trace short). Be careful not to cut adjacent PCB traces, nor cut too deep into the multi-layer circuit board.

If the cut-trace short on a jumper header is already cut, you can return the MPB to its default setting by installing a user-supplied fabricated jumper.

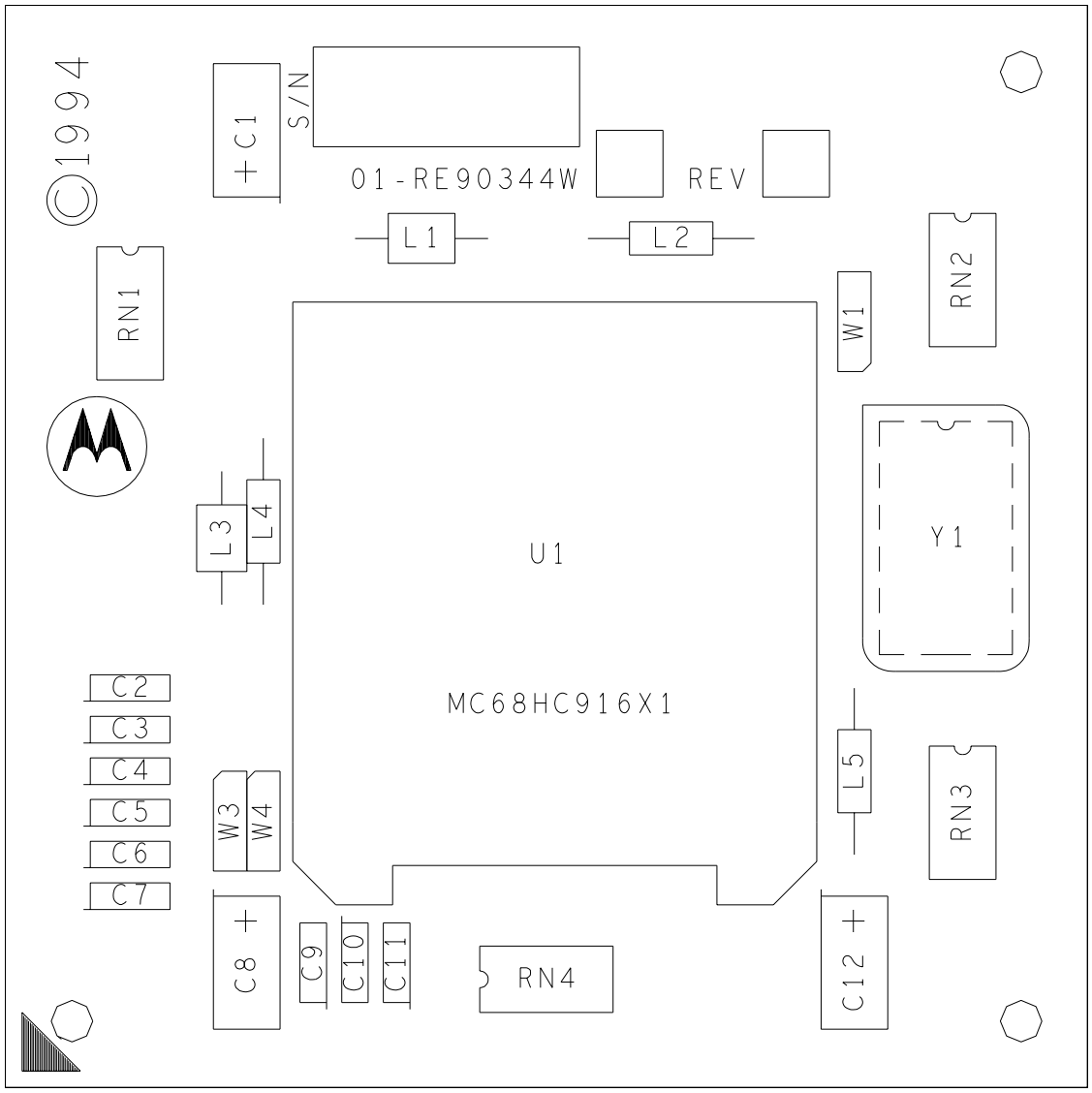

Figure 2-1. MPB Parts Location Diagram (top view)

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Table 2-1. Jumper Header Types

Jumper Header Type	Symbol	Description
two-pin with cut-trace short		Two-pin jumper header with cut-trace short, designated WX, where X = the jumper header number. If you cut the short, use a fabricated jumper to return the jumper header to its factory default state.
three-pin		Three-pin jumper header, designated WX, where X = the jumper header number. Use a fabricated jumper to create a connection between two of the three pins of the jumper header.

Table 2-2. MPB Jumper Header Descriptions

Jumper Header	Type	Description
W1	1 2 3	Jumper between pins 1 and 2 (factory default); selects the MPB on-board crystal clock source. Jumper between pins 2 and 3; selects an external clock source to be the MCU EXTAL input signal.
W2	1 2	Jumper installed or cut-trace short intact (factory default); selects the on-board VDDA power source. No jumper or cut-trace short; enables use of an external power source connected to W2 pin 2. **NOTE** Jumper header W2 is not populated by the factory.
W3	1 2 3	Jumper installed on pins 1 and 2 (factory default); selects the MPB on-board VRH power source. Jumper installed on pins 2 and 3; selects an external VRH power source.
W4	1 2 3	Jumper installed on pins 1 and 2 (factory default); selects the MPB on-board VRL power source. Jumper installed on pins 2 and 3; selects an external VRL power source.

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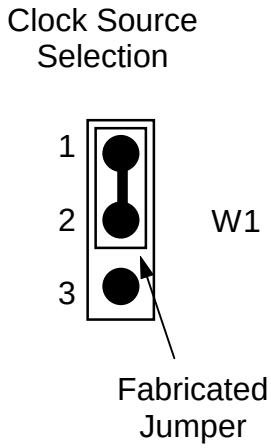
2.2.1 Clock Select Header (W1)

Jumper header W1 connects the MCU external clock (EXTAL) pin to either an on-board or external (target-system) clock source. The drawing below shows the factory configuration: a fabricated jumper on pins 1 and 2. This configuration selects the MPB on-board clock source; crystal oscillator in the Y1 socket. (This crystal provides for operation at the maximum rate the MCU allows via the internal phase-locked loop or direct clock input.)

If you install the MPB in the active probe or directly on a target system, and use the target system clock as the MPB clock, move the fabricated jumper to W1 pins 2 and 3. This connects the MCU EXTAL pin to the MAPI bus input pin. The frequency of the external clock signal can be from 32 KHz to 16.78 MHz (or to the maximum the MCU allows).



NOTE

You cannot drive the MPB clock circuit from an external source (target system) with a discrete crystal. If you use a target system clock source to drive the MPB clock circuit, always use a logic-driven clock such as a hybrid oscillator.

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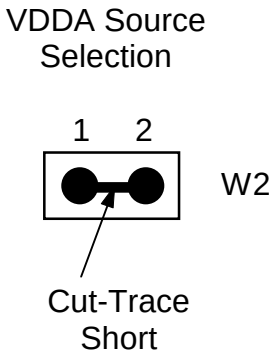
2.2.2 VDDA Select Header (W2)

Jumper header W2 selects the MPB VDDA power source: either MPB power (VDDI) or an external source. The drawing below shows the factory configuration: a cut-trace short between pins 1 and 2. This configuration connects filtered VDDI to VDDA.

To use an external power source, remove the cut-trace short from W2 pins 1 and 2, then connect the external power source to W2 pin 2. Removal of the cut-trace short isolates the MCU VDDA pin from the other MPB circuitry. Isolation lets you connect a precision VDDA source for accurate 10-bit analog/digital (A/D) generation. When connecting an external VDDA power supply to the MPB, connect the power supply ground to insertion point E1. For more information on A/D generation refer to the Analog-To-Digital Converter Reference Manual, ADCRM/AD.



NOTES

If the cut-trace short has been cut, you must install a fabricated jumper on W2 to return it to the factory configuration.

Jumper header W2 is not populated by the factory.

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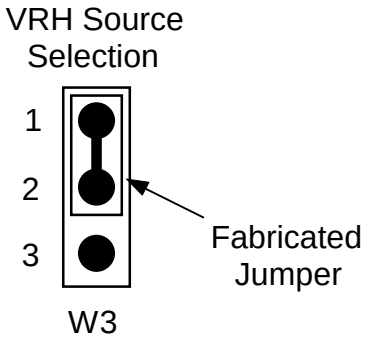
2.2.3 Voltage Reference High Select Header (W3)

Jumper header W3 selects the voltage reference high (VRH) source: either MPB power (VDDA) or an external VRH source. The drawing below shows the factory configuration: a fabricated jumper on pins 1 and 2. This configuration selects VDDA as the VRH source.

To use an external VRH source, first place the fabricated jumper on W3 pins 2 and 3. Then connect the MCU VRH pin to the external VRH source. Each configuration defines the best method for connecting the MCU VRH pin to the external VRH source:

- **MPB/MPFB** – connect via the MPFB logic analyzer connector (refer to Chapter 4 for the appropriate logic analyzer pin).
- **MPB/MMDS1632** – connect via the VRH pin of the target MCU socket
- **MPB/Target System** – connect via the VRH pin of the target system MAPI bus

Alternately, you may remove the jumper and wire-wrap directly to W3 pin 2. Connecting directly to pin 2 is an option regardless of the configuration.



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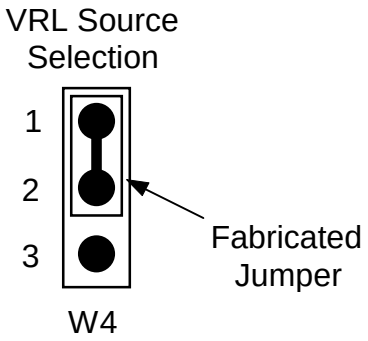
2.2.4 Voltage Reference Low Select Header (W4)

Jumper header W4 selects the voltage reference low (VRL) source: either MPB power (VSSA) or an external VRL source. The drawing below shows the factory configuration: a fabricated jumper on pins 1 and 2. This configuration selects VSSA as the VRL source.

To use an external VRL source, first place the fabricated jumper on W4 pins 2 and 3. Then connect the MCU VRL pin to the external VRL source. Each configuration defines the best method for connecting the MCU VRL pin to the external VRL source:

- **MPB/MPFB** – connect via the MPFB logic analyzer connector (refer to Chapter 4 for the appropriate logic analyzer pin).
- **MPB/MMDS1632** – connect via the VRL pin of the target MCU socket
- **MPB/Target System** – connect via the VRL pin of the target system MAPI bus

Alternately, you may remove the jumper and wire-wrap directly to W4 pin 2. Connecting directly to pin 2 is an option regardless of the configuration.



2.2.5 VSSA Insertion Point (E1)

Insertion point E1 is a plate through hole that lets you connect an external ground to the MPB VSSA pin (refer to paragraph 2.2.2). Insert an external ground wire in E1 and solder it into the plate through hole.

NOTE

Insertion point E1 is not populated by the factory.

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2.3 ANALOG/DIGITAL CIRCUITS

Analog-to-digital (A/D) signals on the MPB are filtered via an installed capacitor (Figure 2-2 is a representative diagram). If your target board also has A/D filter capacitors you must remove either the capacitors on your board or on MPB. Refer to the table below when removing MPB filter capacitors from its associated A/D signal.

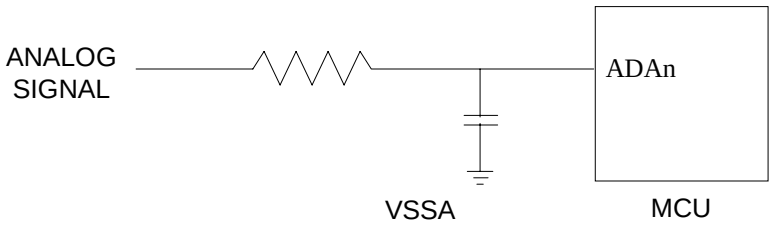

Figure 2-2. A/D Signal Filtering

Signal	Capacitor
AN0	C7
AN1	C5
AN2	C3
AN3	C6
AN4	C4
AN5	C2

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2.4 MEVB CONFIGURATION

The MEVB contains:

- MPB – MCU-device-specific board that defines the MCU to be evaluated.
- M68MPFB1632 Modular Platform Board (MPFB) – which provides the interface connections to the host computer, logic analyzer connections, and the platform for installing the MPB. For more information about the MPFB and MEVB system connections refer to the M68MPFB1632 Modular Platform Board User's Manual, M68MPFB1632/D. Chapter 3 contains information to help you get started using your MEVB.

CAUTION

Turn OFF MPFB power when installing the MPB on the MPFB or removing the MPB from the MPFB. Sudden power surges could damage MEVB integrated circuits.

To install the MPB on the MPFB (refer to Figure 2-3):

1. Inspect all connectors for bent or damaged pins.
2. Align the MPB reference mark with the MPFB reference mark.
3. Rotate the MPB until the four MAPI bus connectors on its bottom mate with the MAPI bus connectors on the top of the MPFB. (There is only one way to connect the MPB and the MPFB.)
4. Firmly press the MPB onto the MPFB.
5. Follow the instructions in the appropriate manual when connecting your debugger hardware to the background debug mode connector.

CAUTION

Support the bottom side of MPFB when installing the MPB on the MPFB. Excessive flexing of the MPFB could damage the printed circuit.

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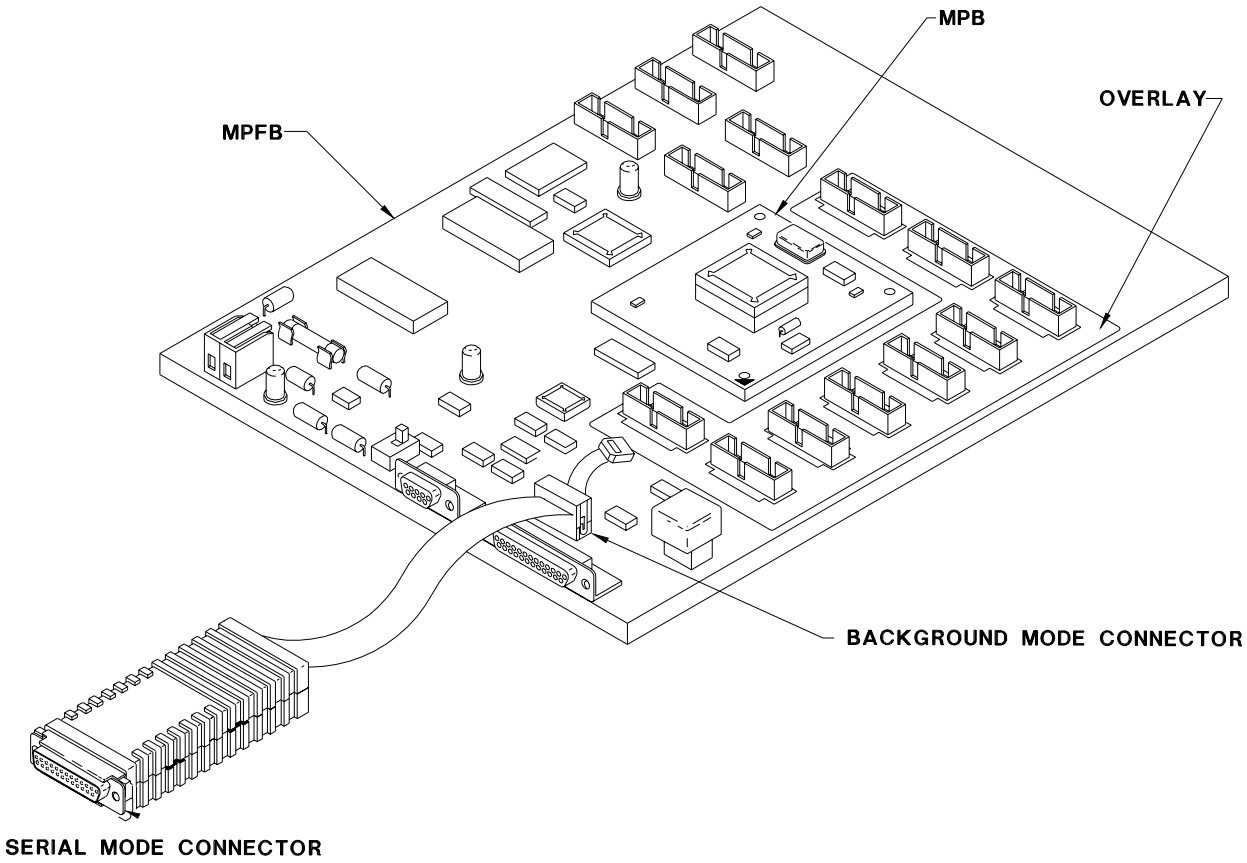

Figure 2-3. MPB – MPFB Interconnection (with serial interface)

After you have installed the MPB, install the plastic overlay on the MPFB: place the overlay over logic analyzer connectors J12 through J20 and press down. Holes in the overlay slide down over plastic clips on the MPFB. These clips hold the overlay in place.

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2.5 ACTIVE PROBE CONFIGURATION

The MMDS1632 Motorola Modular Development System (MMDS) consists of the station module and an active probe. The active probe consists of a three board set, two cables, and a box:

- MPB – MCU-device-specific board that defines the MCU to be evaluated.
- Target Control Board (TCB) – the interface between the MPB, target system, and the station module. The TCB comes with the MMDS. For more information about the TCB refer to the MMDS1632 Motorola Modular Development System User's Manual, MMDS1632UM/D.
- Package Personality Board (PPB) – the board that connects the active probe to the target system. The PPB must be purchased separately. For more information about the PPB refer to the appropriate PPB configuration guide.
- Active probe cables (2) – the interface between the active probe and the station module. 01-RE90340W01 REV 0 and 01-RE90341W01 REV 0 are printed on the active probe cables. The active probe cables come with the TCBe. For more information about the active probe cables refer to the MMDS1632 Motorola Modular Development System User's Manual, MMDS1632UM/D.
- Active probe box – the protective enclosure for the TCB.

CAUTION

Turn off MMDS and target system power when installing or removing MMDS components. Sudden power surges could damage MMDS and target system integrated circuits.

To configure an active probe (refer to Figure 2-4):

1. Inspect all connectors for bent or damaged pins.
2. Rotate the MPB until the four MAPI bus connectors on its bottom mate with the MAPI bus connectors on the top of the TCB. (There is only one way to connect the MPB and the TCB.)
3. Firmly press the MPB and the TCB together.

   Rotate the PPB until the four MAPI bus connectors on its top mate with the MAPI bus connectors on the bottom of the TCB. (There is only one way to connect the PPB and the TCB.)
4. Firmly press the PPB and the TCB together.

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5. Connect one end of the 01-RE90341W01 REV 0 active probe cable to connector P6 on the MMDS control board; connect the other end to connector J6 on the TCB. Connect one end of the 01-RE90340W01 REV 0 active probe cable to connector P5 on the MMDS control board; connect the other end to connector J5 on the TCB. Secure the connector clamps on TCB connectors J5 and J6.

The active probe is now ready to connect to the target system (refer to the PPB configuration guide for information on connecting the active probe to the target system.)

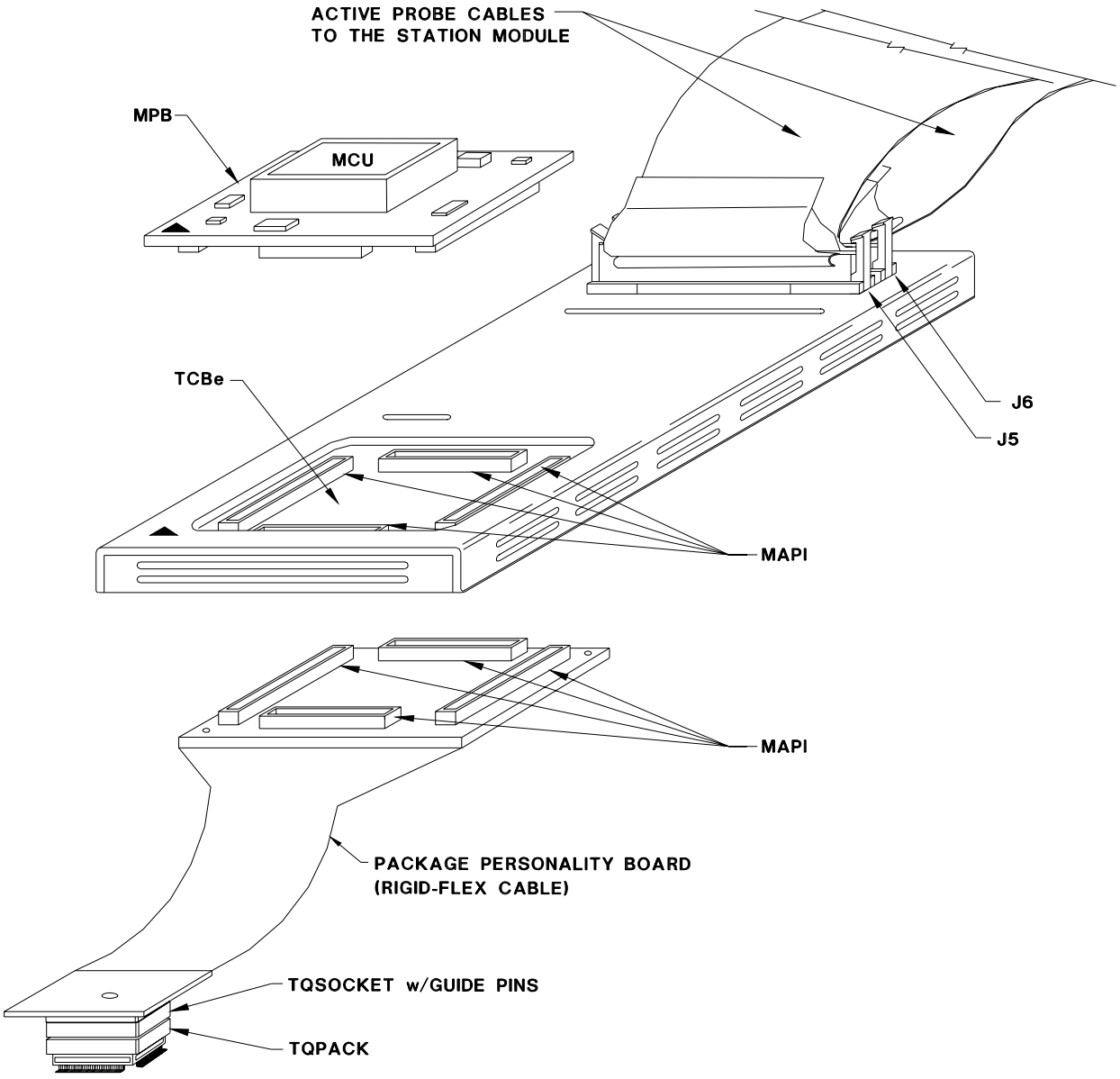

Figure 2-4. Active Probe Interconnection (with Active Probe Box)

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CHAPTER 3
MEVB QUICK START GUIDE

3.1 INTRODUCTION

This quick start guide is intended for the user who may not be familiar with Motorola's development tools. This chapter explains the MEVB hardware and software setup for M68MEVB916X1 operation. Hardware setup consists of configuring the MPB and MPFB jumper headers; software setup consists of running the appropriate initialization code within the debugger.

For the purpose of this quick start guide the MPB jumper headers should be configured in their default positions. Chapter 2 of this manual contains the default jumper header settings for the MPB.

3.2 CONFIGURING THE MPFB

The MPFB includes jumper-selectable options such as chip select usage, memory type selection and memory size selection for the pseudo ROM sockets, and reset data control.

NOTE

The MPFB must be configured for the specific MPB. Paragraph 3.2.2 provides a configuration for basic MPFB operation. For a detailed description of the MPFB jumper header selections refer to the M68MPFB1632 Modular Platform Board User's Manual, M68MPFB1632/D.

3.2.1 MPFB Memory Devices

Pseudo ROM refers to memory locations U2 & U4. The two pseudo ROM sockets are generic memory sockets that accept a variety of RAM, EPROM, or EEPROM devices. The pseudo ROM sockets, as shipped from the factory, contain two 32K x 8 RAM devices. These memories are 28-pin package devices.

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3.2.2 MPFB Jumper Headers

Configure your MPFB jumper headers per the instructions in Table 3-1. Table 3-1 contains information exclusively intended for quick start and ignores the other jumper headers.

Table 3-1. MPFB Quick Start Jumper Header Configuration

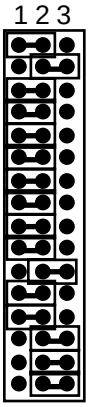
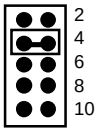
Jumper Header	Type	Description
W2		Install a jumper on pins 1 and 2 to configure pin 1 of the memory devices in the pseudo ROM sockets (U2 & U4) as a standard address line.
W3		Install a jumper on pins 1 and 2 to indicate that the memory devices in the pseudo ROM sockets (U2 & U4) have 28 pins.
W4		Install a jumper on pins 1 and 2 to set the pseudo ROM port size (memory data width) as word.
W5		Install a jumper on pins 2 and 3 to enable the PRU.
W6		W6 selects the MCU operation mode. Each 3-pin jumper header set corresponds to an MCU data line. While the reset pin is low, the reset data values are driven on the data bus (D0 – D15). (The MEVB reset data circuit is open drain; a high state is provided via a pull-up resistor.) Each reset data line may be set high (H) or low (L). Consult the appropriate MCU user's manual, data book, or technical summary for reset data information.
W10		Install a jumper on pins 1 and 2 to indicate that RAM is installed in the pseudo ROM sockets (U2 & U4).
W12		Install a jumper on pins 3 and 4 to indicate that the two devices installed in the pseudo ROM sockets (U2 & U4) are 32K x 8.

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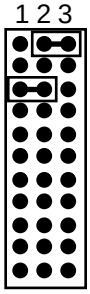
Table 3-1. MPFB Quick Start Jumper Header Configuration (continued)

Jumper Header	Type	Description
W14	1 2 3 	Jumper header W14 selects the MCU signal for the memory devices in the fast RAM sockets (U9 & U10) and pseudo ROM sockets (U2 & U4). Pins 1 and 2 select the MCU chip select for the memory devices in the fast RAM sockets. Pins 2 and 3 of jumper header W14 select the chip select for the memory devices in the pseudo ROM sockets. Jumper installed on CSBOOT pins 2 and 3 (factory default); use CSBOOT as the memory device chip enable for memory devices in the pseudo ROM sockets.
W16	1 2	No jumper installed; the MCU MODCLK signal is pulled high (logic 1) via a resistor during reset.
W17	1 2	No jumper installed; the BERR signal is pulled high (logic 1) via a resistor during reset.
W18	1 2 3	Install a jumper on pins 1 and 2 for unrestricted writes to the memory devices in the pseudo ROM sockets (U2 & U4).
W19	1 2 3	Install a jumper on pins 1 and 2 to ground the A19 signal to the MPFB memory arrays.
W22	1 2 3	Install a jumper on pins 2 and 3 to select the evaluation MCU (on the MPB) as an M68HC16 MCU device.

3.3 MEVB INSTALLATION INSTRUCTIONS

MEVB installation requires a user-supplied power supply and host computer. The host computer must have the appropriate I/O port (serial or parallel) as required by your debugger hardware; as well as the appropriate operating system as required by your debugger software (refer to the appropriate debugger documentation for these requirements). The following paragraphs explain MPFB connections. Refer to Chapter 2 for instructions to connect the MPB and MPFB.

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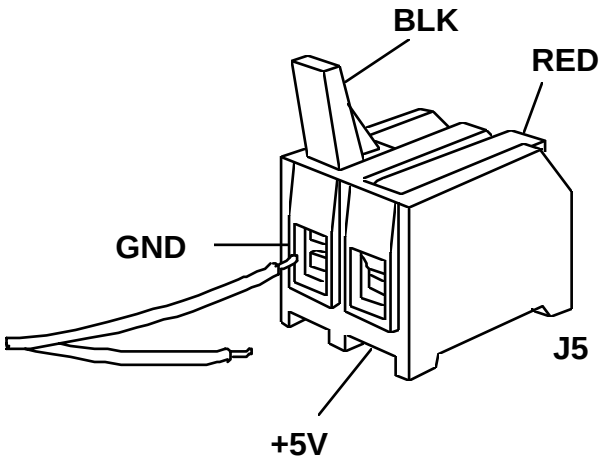
3.3.1 Power Supply – MPFB Connection

Use MPFB connector J5 to connect a user-supplied power supply to the MEVB. Contact 1 is ground; black lever. Contact 2 is VDD (+5 volts); red lever. Use 20 or 22 AWG wire for power connections. For each wire, trim back the insulation 1/4 in. (.635 cm), lift the appropriate lever of J5 to release tension on the contacts, then insert the bare wire into J5 and close the lever. The MEVB requires a +5Vdc @ 1.0 amp power supply for operation. A 1.5 amp fuse is installed on the MPFB +5Vdc power supply input line.



CAUTIONS

Do not use wire larger than 20 AWG in connector J5. Such wire could damage the connector.

Turn off MEVB power when installing or removing the MPB from the MPFB. Sudden power surges could damage MEVB integrated circuits.

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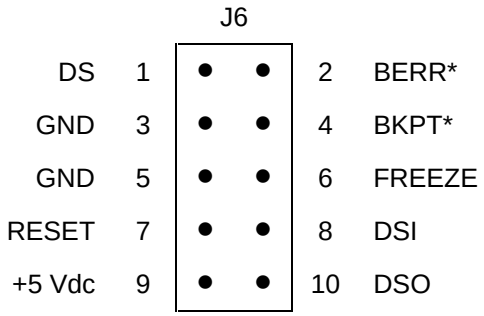
3.3.2 Personal Computer – BDM Connection

Personal computer communication with the MEVB requires background debug mode (BDM) hardware. Connect your BDM hardware between your computer's I/O port and the BDM header on the MPFB (MPFB connector J6). The drawing below shows signal assignments for connector J6. For additional information about your BDM software/hardware, including debugging and assembly information, see the appropriate user's manual.



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3.4 SOFTWARE INSTALLATION

After you have set up the MEVB hardware you must install ICD16 in your computer. To install the software and initialize your MEVB:

1. Insert the software diskette into the 3.5-inch drive of your computer.
2. Type the drive letter, followed by the word `install`. For example, if your 3.5-inch drive is drive B, type: **`b install`**
3. The install program automatically loads the software. Follow the instructions that appear on the screen. This completes software loading.
4. After you have configured the MEVB hardware and installed ICD16 on your hard drive, turn on the MEVB power supply.
5. To start ICD type:

   `C:/>`**`ICD16 [option] [option]`** Use the correct pathname to access ICD16

`[option]`	*ICD optional parameters are:*
`bw`	*Set display to black and white*
`lpt1`	*Use lpt1 (default)*
`lpt2`	*Use lpt2*
`lpt3`	*Use lpt3*
`-or-`	
`path`	*A DOS path to directory containing the source code for source level debug.*

   Example: ICD16 bw lpt2 If more than one option is given, they must be separated by spaces.

6. To install macros from the ICD16 debugger, type at the ICD16 debug window prompt:

   >macs

   This command opens a window containing a list of macros with the .ICD extension. Use the arrow keys to highlight and the <return> key to select the initialization macro: MPBX1.ICD. MPBX1.ICD sets up the MEVB for basic operation. The macro file enables the maximum system clock frequency and disables the software watchdog while enabling the bus monitor. CSBOOT is set to zero-wait state and the block size set to 64K starting at $00000. The SRAM is enabled to reside at $10000 with the stack pointer initialized at $103FE and the instruction pointer (IP) initialized to $00200 (PK=0, IP=200).
7. Load your program at address $00200.

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Below is the MPBX1.ICD initialization macro program listing.

```
symbol SCIMCR FFA00
symbol SYNCR FFA04
symbol SYPCR FFA21
symbol CSBARBT FFA48
symbol CSORBT FFA4A
symbol START 00200
dmmw SCIMCR 40CF        Set module mapping to $FFF000-$FFFFFF
dmmb SYNCR 7F           Set system clock frequency to 16.78 MHz
dmmb SYPCR 04           Turn off software watchdog timer
dmmw CSBARBT 0003       Change CSBOOT block size to 64K
dmmw CSORBT 7830        Change wait state to zero
mdf6 START              Display program in PMM window
pk=0                    Initialize CPU registers
a=AA
b=BB
e=0000
ix=0000
iy=0000
iz=0000
hr=0000
ir=0000
k=0000
sp=03fe                 Initialize the stack pointer
sk=1
symbol TRAMBAR FFB04
symbol TRAMMCR FFB00
dmmb TRAMBAR 01         Set SRAM base address
dmmb TRAMMCR 00         Enable SRAM array
dmml 10000 4D6F746F     Check SRAM: write Motorola 68HC16 advanced MCUs
dmml 10004 726F6C61
dmml 10008 20363848
dmml 1000C 43313620
dmml 10010 41647661
dmml 10014 6E636564
dmml 10018 20204D43
dmml 1001C 55732020
dmml 10020 36384843
mdf3 10000              Display SRAM in DMM window
ip=START                Start entering your program here
```

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CHAPTER 4
MEVB SUPPORT INFORMATION

4.1 INTRODUCTION

This chapter's information is pertains to using the MPB in an MEVB (the MPB installed on a MPFB). Signals on the MPFB logic analyzer connectors are defined by the MPB type.

4.2 LOGIC ANALYZER CONNECTOR SIGNALS

The tables of this chapter describe MPFB logic analyzer connector signals if you install an M68MPB916X1 on the MPFB. The signal descriptions on J12 – J20 are the logic analyzer pin-outs on the plastic overlay supplied with the MPB.

NOTE

The signal descriptions in the following tables are for quick reference only. The MC68HC916X1 User's Manual, MC68HC916X1UM/AD, contains a complete description of the MC68HC916X1 MCU signals.

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Table 4-1. Logic Analyzer Connector J7 Pin Assignments

PIN	MNEMONIC	SIGNAL
1, 2	SPARE	No connection
3	OE(ALL)	I/O PRU OUTPUT ENABLE – Input, active high; when low disables *all* PRU outputs.
4 – 11	PEPAR7 – PEPAR0	PEPAR OUTPUTS – Output signals that show the *complement* (negated contents) of the PEPAR register.
12 – 19	PE7 – PE0	PORT E I/O SIGNALS – PRU replacement of the port E function.
20	GND	GROUND

Table 4-2. Logic Analyzer Connector J8 Pin Assignments

PIN	MNEMONIC	SIGNAL
1, 2	SPARE	No connection
3	OE(ABG)	I/O PRU OUTPUT ENABLE – Input, active high; when low disables port A, port B, and port G outputs.
4 – 11	PA7 – PA0	PORT A I/O SIGNALS – PRU replacement of the port A function.
12 – 19	PB7 – PB0	PORT B I/O SIGNALS – PRU replacement of the port B function.
20	GND	GROUND

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Table 4-3. Logic Analyzer Connector J9 Pin Assignments

PIN	MNEMONIC	SIGNAL
1, 2	SPARE	No connection
3	OE(H)	I/O PRU OUTPUT ENABLE – Input, active high; when low disables the port H outputs.
4 – 11	PH7 – PH0	PORT H I/O SIGNALS – PRU replacement of the port H function.
12 – 19	PG7 – PG0	PORT G I/O SIGNALS – PRU replacement of the port G function.
20	GND	GROUND

Table 4-4. Logic Analyzer Connector J10 Pin Assignments

PIN	MNEMONIC	SIGNAL
1	+5V	+5 VDC POWER – Input voltage (+5 Vdc @ 1.0 A) used by the MEVB logic circuits. (To make this pin no connection, remove the jumper from the header on the MPFB.)
2	SPARE	No connection
3	AS	ADDRESS STROBE – Active-low output signal that indicates whether a valid address is on the address bus.
4 – 19	A15 – A0	ADDRESS BUS BITS 15 – 0 – Sixteen bits of the 24-bit address bus.
20	GND	GROUND

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Table 4-5. Logic Analyzer Connector J11 Pin Assignments

PIN	MNEMONIC	SIGNAL
1	+5V	+5 VDC POWER – Input voltage (+5 Vdc @ 1.0 A) used by the MEVB logic circuits. (To make this pin no connection, remove the jumper from the header on the MPFB.)
2	SPARE	No connection
3	DS	DATA STROBE – Active-low output signal. During a read cycle, indicates that an external device should place valid data on the data bus. During a write cycle, indicates that valid data is on the data bus.
4 – 19	D15 – D0	DATA BUS 15 – 0 – 16 bits of the MCU bi-directional data bus lines.
20	GND	GROUND

Table 4-6. Logic Analyzer Connector J12 Pin Assignments

PIN	MNEMONIC	SIGNAL
1, 2	SPARE	No connection
3	CLKOUT	SYSTEM CLOCK OUT – Output signal that is the MCU internal system clock.
4	BERR	BUS ERROR – Active-low signal that indicates a memory access error has occurred.
5	BKPT /	BREAKPOINT – Active-low input signal that signals a hardware breakpoint to the CPU.
	DSCLK	Development Serial Clock – Clock input signal for background debug mode.
6	FREEZE	FREEZE – Output signal that indicates the CPU has acknowledged a breakpoint.
	QUOT	QUOTIENT OUT – Output signal that furnishes the quotient bit of the polynomial divider for test purposes.
7	LAT-DSO / (Latched IPIPE0)	LATCHED INSTRUCTION PIPE 0 – Latched output signal of the first state of IPIPE0 for CPU16-based MCUs; indicates instruction pipeline activity.

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Table 4-6. Logic Analyzer Connector J12 Pin Assignments (continued)

PIN	MNEMONIC	SIGNAL
8	LAT-DSI (Latched IPIPE1)	LATCHED INSTRUCTION PIPE 1 – Latched output signal of the first state of IPIPE1 for CPU16-based MCUs; indicates instruction pipeline activity.
9	DSO / (IPIPE0)	DEVELOPMENT SERIAL OUT – Serial data output signal for background debug mode. INSTRUCTION PIPE 0 for CPU16-based MCUs.
10	DSI / (IPIPE1)	DEVELOPMENT SERIAL IN – Serial data input signal for background debug mode. INSTRUCTION PIPE 1 for CPU16-based MCUs.
11	DSACK1	DATA AND SIZE ACKNOWLEDGE 1 – Active-low input signal that allows asynchronous data transfers and dynamic bus sizing between the MCU and external devices.
12	PULL-UP	Not connected; pulled high through a resistor on the MPB.
13	FC2 / CS5	FUNCTION CODE 2 – Output signal that identifies the processor state and address space of the current bus cycle. CHIP SELECT 5 – Output signal that selects peripheral or memory devices at programmed addresses.
14	FC1	FUNCTION CODE 1 – Output signal that identifies the processor state and address space of the current bus cycle.
15	FC0 / CS3	FUNCTION CODE 0 – Output signal that identifies the processor state and address space of the current bus cycle. CHIP SELECT 3 – Output signal that selects peripheral or memory devices at programmed addresses.
16	SIZ1	TRANSFER SIZE – Active-high output signals that Indicates the number of bytes to be transferred during a bus cycle.

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Table 4-6. Logic Analyzer Connector J12 Pin Assignments (continued)

PIN	MNEMONIC	SIGNAL
17	SIZ0	TRANSFER SIZE – Active-high output signals that indicates the number of bytes to be transferred during a bus cycle.
18	R/W	READ/WRITE – Active-high output signal that indicates the direction of data transfer on the bus.
19	BGACK /	BUS GRANT ACKNOWLEDGE – Active-low input signal that indicates an external device has assumed bus mastership.
	CSE	EMULATOR CHIP SELECT – Active-low output signal that selects external emulation devices at internally-mapped addresses. CSE is used to emulate I/O ports.
20	GND	GROUND

Table 4-7. Logic Analyzer Connector J13 Pin Assignments

PIN	MNEMONIC	SIGNAL
1	+5V	+5 VDC POWER – Input voltage (+5 Vdc @ 1.0 A) used by the MEVB logic circuits. (To make this pin no connection, remove the jumper from the header on the MPFB.)
2	SPARE	No connection
3	DSACK1	DATA AND SIZE ACKNOWLEDGE 1 – Active-low input signal that allows asynchronous data transfers and dynamic bus sizing between the MCU and external devices.
4, 5	PULL-UP	Not connected; pulled high through a resistor on the MPB.
6	AS	ADDRESS STROBE – Active-low output signal that indicates a valid address is on the address bus.
7	DS	DATA STROBE – Active-low output signal. During a read cycle, indicates that an external device should place valid data on the data bus. During a write cycle, indicates that valid data is on the data bus.

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Table 4-7. Logic Analyzer Connector J13 Pin Assignments (continued)

PIN	MNEMONIC	SIGNAL
8	BR /	BUS REQUEST – Active-low input signal that indicates an external device requires bus mastership.
	CS0	CHIP SELECT 0 – Output signal that selects peripheral or memory devices at programmed addresses.
9	BG /	BUS GRANT – Active-low output signal that indicates the MCU has relinquished the bus.
	CSM	INTERNAL MODULE CHIP SELECT – CSM is not supported on the M68HC916X1 MCU.
10	PULL-UP	Not connected; pulled high through a resistor on the MPB.
11	CLKOUT	SYSTEM CLOCK OUTPUT – MCU internal clock output signal.
12	A23 /	ADDRESS BUS BIT 23 – One bit of the 24-bit address bus.
	CS10	CHIP SELECT 10 – Output signal that selects peripheral or memory devices at programmed addresses.
13 – 15	PULL-UP	Not connected; pulled high through a resistor on the MPB.
16	A19 /	ADDRESS BUS BIT 19 – One bit of the 24-bit address bus.
	CS6	CHIP SELECT 6 – Output signal that selects peripheral or memory devices at programmed addresses.
17 – 19	A18 – A16	ADDRESS BUS 18 – 16 – Three bits of the 24-bit address bus.
20	GND	GROUND

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Table 4-8. Logic Analyzer Connector J14 Pin Assignments

PIN	MNEMONIC	SIGNAL
1, 2	SPARE	No connection
3	PULL-UP	Not connected; pulled high through a resistor on the MPB.
4	MODCLK	CLOCK MODE SELECT – Input signal that configures the MCU internal clock at reset.
5	TSC	THREE STATE CONTROL – When TSC is logic high, this input signal forces all output drivers to a high-impedance state.
6	RESET	RESET – Active-low, bi-directional signal that starts a system reset.
7	PULL-UP	Not connected; pulled high through a resistor on the MPB.
8	SPARE	No connection
9, 10	IRQ6, IRQ7	TARGET INTERRUPT REQUEST 6, 7 - Active-low input signals from the target that asynchronously provides an interrupt priority level to the CPU. IRQ1 has the lowest priority, IRQ7 has the highest.
11 – 15	GND	GROUND
16 – 19	SPARE	No connection
20	GND	GROUND

Table 4-9. Logic Analyzer Connector J15 Pin Assignments

PIN	MNEMONIC	SIGNAL
1 – 3	SPARE	No connection
4 – 17	GND	GROUND
18, 19	SPARE	No connection
20	GND	GROUND

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Table 4-10. Logic Analyzer Connector J16 Pin Assignments

PIN	MNEMONIC	SIGNAL
1 – 4	SPARE	No connection
5 – 12	VSSA	A/D GROUND – A/D ground reference.
13 – 19	SPARE	No connection
20	VSSA	A/D GROUND – A/D ground reference.

Table 4-11. Logic Analyzer Connector J17 Pin Assignments

PIN	MNEMONIC	SIGNAL
1 – 4	SPARE	No connection
5 – 8	VSSA	A/D GROUND – A/D ground reference.
9	VRH	VOLTAGE REFERENCE HIGH – Input reference supply voltage (high) line (must set jumper on the MPB).
10	VRL	VOLTAGE REFERENCE LOW – Input reference supply voltage (low) line (must set jumper on the MPB).
11	AN0	ANALOG INPUT 0 – Analog input line to the MCU device.
12	AN1 – AN5	ANALOG INPUT 1 - 5 – Analog input lines to the MCU device.
17 – 19	SPARE	No connection
20	VSSA	A/D GROUND – A/D ground reference.

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Table 4-12. Logic Analyzer Connector J18 Pin Assignments

PIN	MNEMONIC	SIGNAL
1 – 4	SPARE	No connection
5 – 13	GND	GROUND
14 – 16	IC1 – IC3	INPUT CAPTURE 1 - 3 – Input signals that latch the contents of the GPT timer counter (TCNT) into the input capture registers TIC1 - TIC3 when a selected edge occurs at the pin.
17 – 19	SPARE	No connection
20	GND	GROUND

Table 4-13. Logic Analyzer Connector J19 Pin Assignments

PIN	MNEMONIC	SIGNAL
1 – 4	SPARE	No connection
5 – 8	OC1 – OC4	OUTPUT COMPARE 1 - 4 – Output signals that are generated when the GPT timer counter (TCNT) and TOC1 - TOC4 comparator registers contain the same value.
9	IC4 /	INPUT CAPTURE 4 – Input signal that latches the contents of the GPT timer counter (TCNT) into the input capture register TI4O5 when a selected edge occurs at the pin.
	OC5	OUTPUT COMPARE 5 – Output signal that is generated when the GPT timer counter (TCNT) and TI4O5 comparator register contain the same value.
10, 11	PWMA, PWMB	PULSE WIDTH MODULATION A and B – Repetitive output signals whose high time to low time ratio can be controlled by the CPU.
12	PAI	PULSE ACCUMULATOR INPUT – Input signal that increments an 8-bit counter.
13 – 19	SPARE	No connection
20	GND	GROUND

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Table 4-14. Logic Analyzer Connector J20 Pin Assignments

PIN	MNEMONIC	SIGNAL
1 – 4	SPARE	No connection
5 – 8	GND	GROUND
9	MISO	MASTER-IN, SLAVE-OUT – Serial input to SPI in master mode; serial output from SPI in slave mode.
10	MOSI	MASTER-OUT, SLAVE-IN – Serial output from SPI in master mode; serial input to SPI in slave mode.
11	SCK	SPI SERIAL CLOCK – In master mode, the clock signal from the SPI; in slave mode the clock signal to the SPI.
12	PCS0 / SS	PERIPHERAL CHIP SELECT 0 – Active-low output SPI peripheral chip select signal. SLAVE SELECT – Bi-directional, active-low signal that initiates serial transmission when SPI is in slave mode; causes mode fault in master mode.
13 – 15	PCS1 – PCS3	PERIPHERAL CHIP SELECT 1 – 3 – Active-low output SPI peripheral chip select signal.
16	RXD	RECEIVE DATA – RS-232C serial data input line.
17	TXD	TRANSMIT DATA – Serial data output line.
18	PCLK	AUXILIARY TIMER CLOCK INPUT – External input clock source to the GPT.
19	SPARE	No connection
20	GND	GROUND

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CHAPTER 5

MAPI SUPPORT INFORMATION

5.1 INTRODUCTION

This chapter information pertains to installing the MPB on a target system. The figures in this chapter show the MAPI interface connector layout and pin assignments for MPB connectors P1, P2, P3, and P4 (Figures 5-1 through 5-5).

5.2 MAPI BUS CONNECTORS

The connectors required to interface to the MAPI bus are:

2	Robinson Nugent	2 X30 plugs	P50L-060P-AS-TGF
2	Robinson Nugent	2 X40 plugs	P50L-080P-AS-TGF

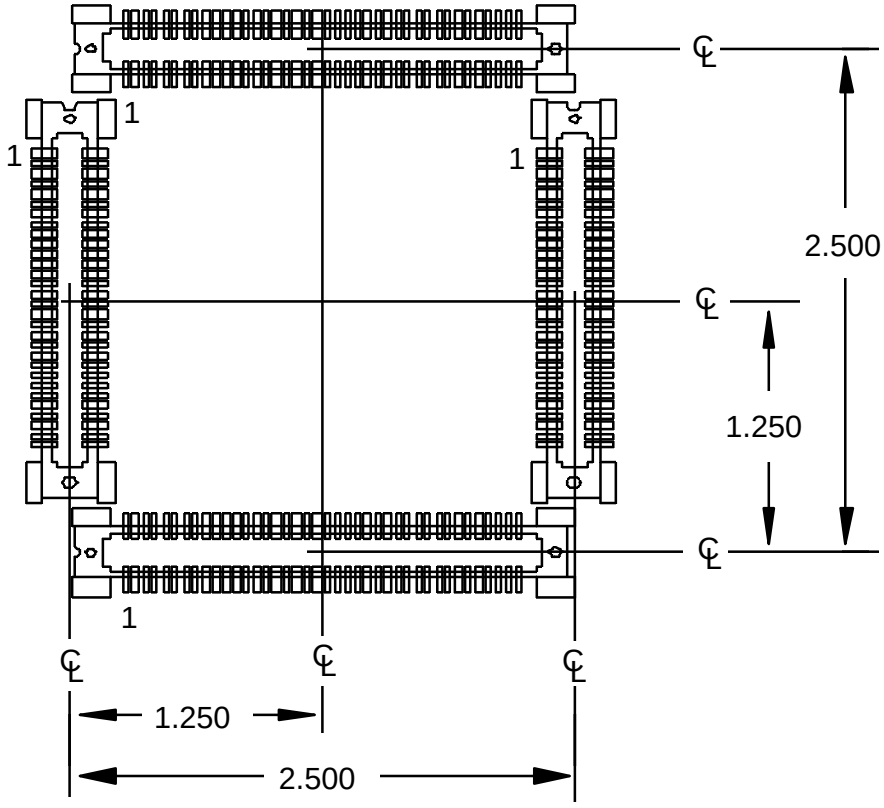

Figure 5-1. MAPI Interface Connector Layout

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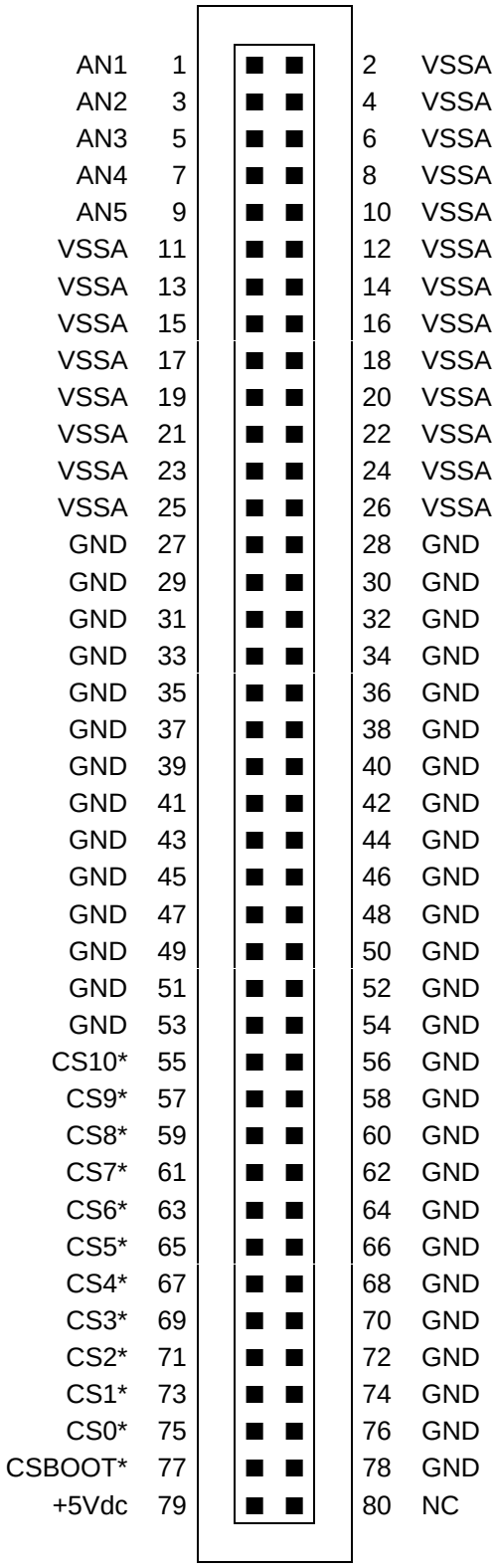
AN1 1 2 VSSA
AN2 3 4 VSSA
AN3 5 6 VSSA
AN4 7 8 VSSA
AN5 9 10 VSSA
VSSA 11 12 VSSA
VSSA 13 14 VSSA
VSSA 15 16 VSSA
VSSA 17 18 VSSA
VSSA 19 20 VSSA
VSSA 21 22 VSSA
VSSA 23 24 VSSA
VSSA 25 26 VSSA
GND 27 28 GND
GND 29 30 GND
GND 31 32 GND
GND 33 34 GND
GND 35 36 GND
GND 37 38 GND
GND 39 40 GND
GND 41 42 GND
GND 43 44 GND
GND 45 46 GND
GND 47 48 GND
GND 49 50 GND
GND 51 52 GND
GND 53 54 GND
CS10* 55 56 GND
CS9* 57 58 GND
CS8* 59 60 GND
CS7* 61 62 GND
CS6* 63 64 GND
CS5* 65 66 GND
CS4* 67 68 GND
CS3* 69 70 GND
CS2* 71 72 GND
CS1* 73 74 GND
CS0* 75 76 GND
CSBOOT* 77 78 GND
+5Vdc 79 80 NC

Figure 5-2. MAPI Interface Connector P1 Pin Assignments

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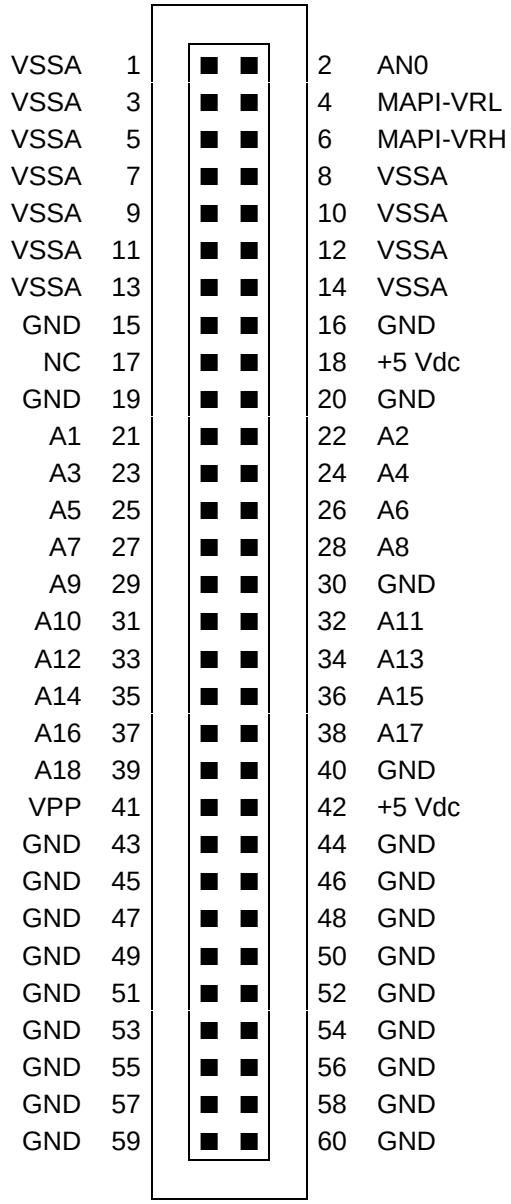

Figure 5-3. MAPI Interface Connector P2 Pin Assignments

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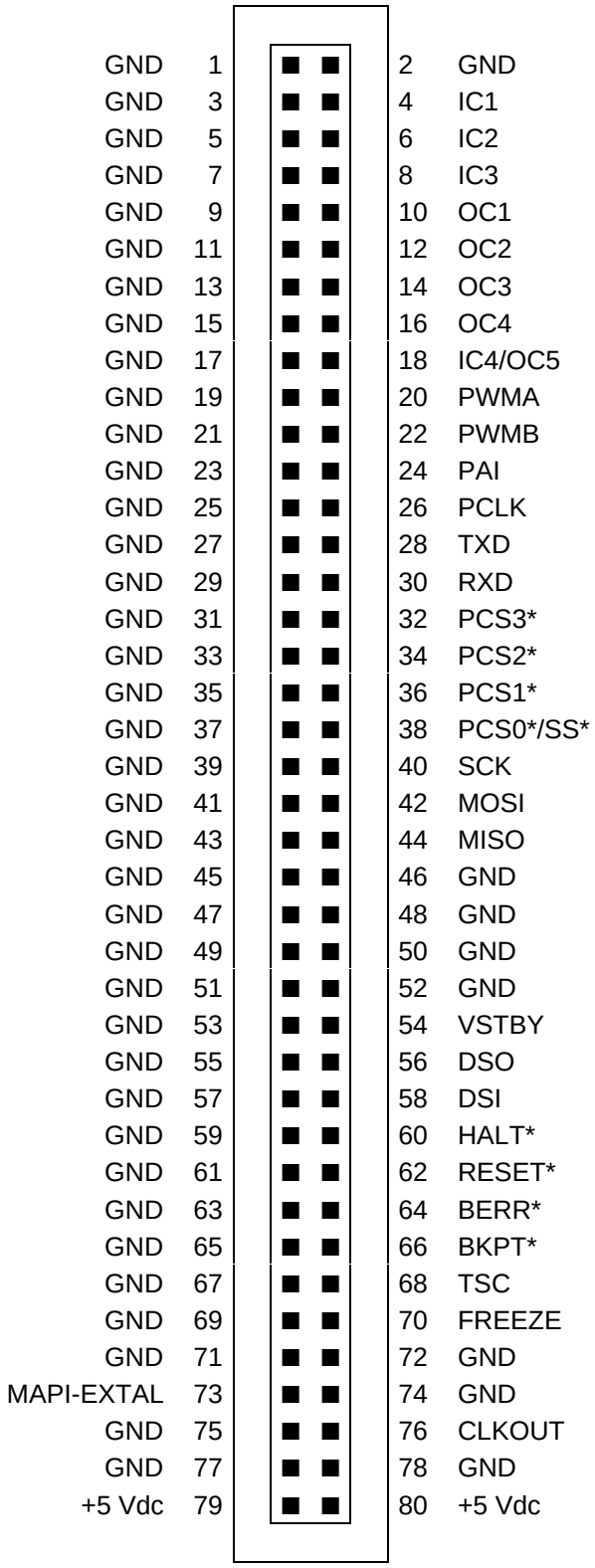

Figure 5-4. MAPI Interface Connector P3 Pin Assignments

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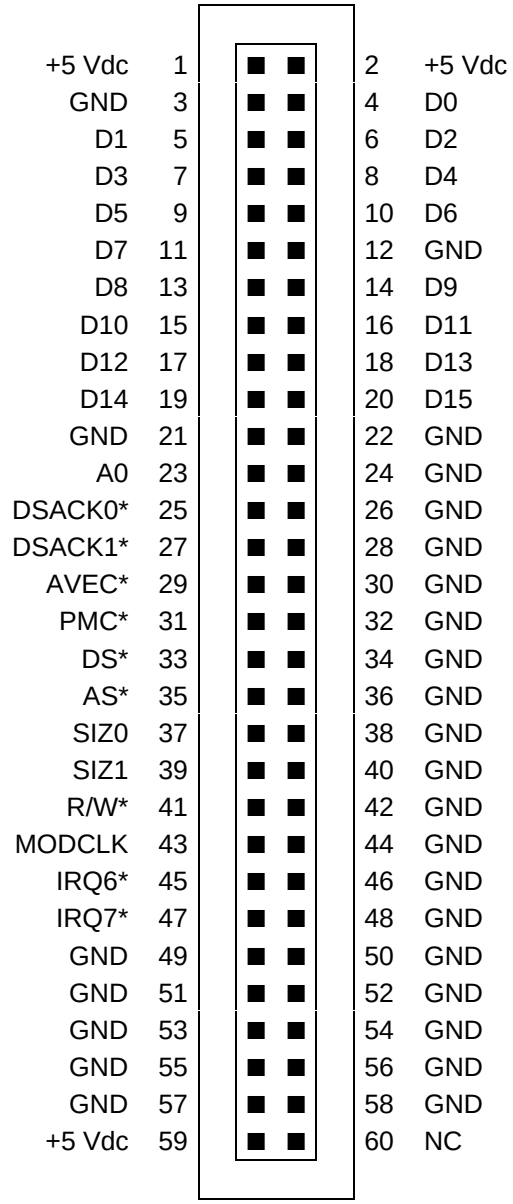

Figure 5-5. MAPI Interface Connector P4 Pin Assignments

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CHAPTER 6
SCHEMATIC DIAGRAMS

6.1 INTRODUCTION

This chapter contains the M68MPB16Y1 MCU Personality Board (MPB) schematic diagrams. These schematic diagrams are for reference only and may deviate slightly from the circuits on your MPB.

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TABLE OF CONTENTS

1	TITLE & REVISION STATUS
2	NOTES
3	BYPASS CAPACITORS, CLEAN POWER & SIGNAL FILTERS
4	MODULAR ACTIVE PROBE INTERCONNECT P1 & P3
5	MODULAR ACTIVE PROBE INTERCONNECT P2 & P4
6	MCU & CLOCK
7	PULLUPS/PULLDOWNS/PERSONALITY ID
8	SIGNAL CROSS REFERENCES

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED
	0	ORIGINAL RELEASE	10/05/92	R.E.
	A	REMOVED RC FILTER FROM A/D, CHANGED INDUCTOR SIZE, TANTALUM CAP VOLTAGES.	09/09/94	

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DRAWN BY: R.E. DATE: 10/05/92

DESIGN ENGINEER: R.E. DATE: 10/05/92

PROJECT LEADER: R.E. DATE: 10/05/92

MOTOROLA INC.
MICROPROCESSOR AND MEMORY TECHNOLOGIES GROUP
6501 WILLIAM CANNON DRIVE WEST AUSTIN, TEXAS 78735 USA

TITLE: SCHEMATIC - MPB916X1C

SIZE: A | GEDTTL: BOARD | GEDABV: MPB916X1C | DWG. NO. 63ASE90344W | REV: A

LAST_MODIFIED=Fri Sep 9 11:29:14 1994

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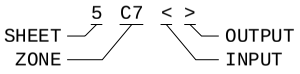
NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS, 5%, 1/8 WATT.
   ALL CAPACITORS ARE IN UF. 50V.
   ALL VOLTAGES ARE DC.
2. INTERRUPTED LINES CODED WITH THE SAME LETTER OR LETTER COMBINATIONS ARE ELECTRICALLY CONNECTED.
3. DEVICE TYPE NUMBER IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH THE MANUFACTURER.
4. SPECIAL SYMBOL USAGE:
   * DENOTES - ACTIVE LOW SIGNAL.
   <> DENOTES - VECTORED SIGNALS.
5. INTERPRET DIAGRAM IN ACCORDANCE WITH AMERICAN NATIONAL STANDARDS INSTITUTE SPECIFICATIONS, CURRENT REVISION, WITH THE EXCEPTION OF LOGIC BLOCK SYMBOLOGY.
6. CODE FOR SHEET TO SHEET REFERENCES IS AS FOLLOWS:



7. VCC LOCATIONS
   UNLESS OTHERWISE SPECIFIED, VCC IS APPLIED TO:
   PIN 8 OF ALL 8-PIN ICS
   PIN 14 OF ALL 14-PIN ICS
   PIN 16 OF ALL 16-PIN ICS
   PIN 20 OF ALL 20-PIN ICS, ETC.
8. GROUND LOCATIONS
   UNLESS OTHERWISE SPECIFIED, GROUND IS APPLIED TO:
   PIN 4 OF ALL 8-PIN ICS
   PIN 7 OF ALL 14-PIN ICS
   PIN 8 OF ALL 16-PIN ICS
   PIN 10 OF ALL 20-PIN ICS, ETC.

NOTES

SIZE		DWG. NO.	REV:
A	GEDTTL: BOARD GEDABV: MPB916X1C	63ASE90344W	A
LAST_MODIFIED=Fri Sep 9 10:44:58 1994		SHEET 2 OF 8	

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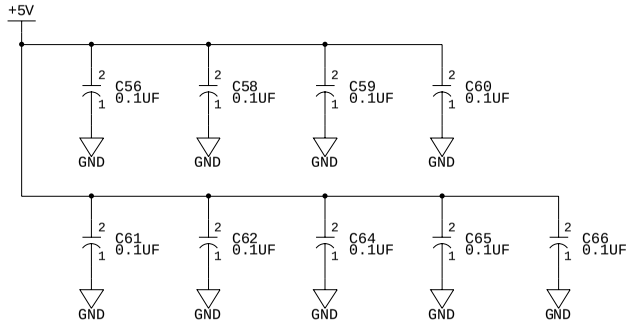
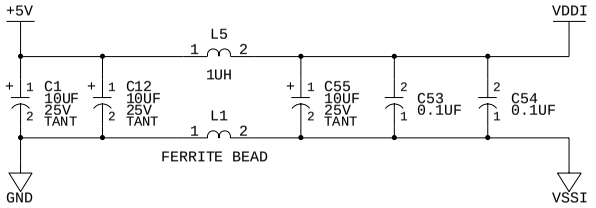
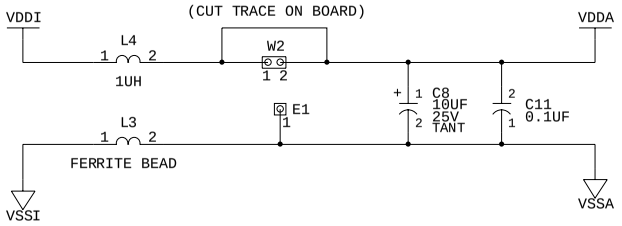
+5V AND GND DECOUPLING
FOR VDDE OF MCU AND OSCILLATOR



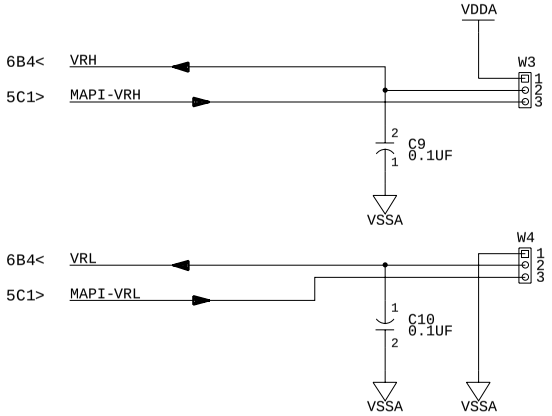
VDDI/VSSI GENERATION



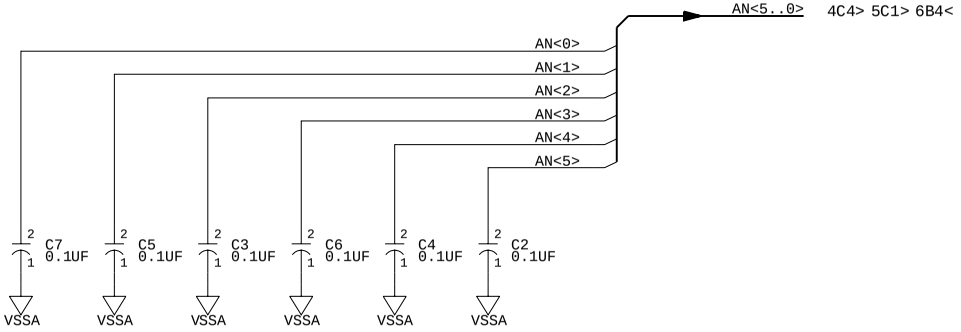
ADC MODULE
VDDA/VSSA GENERATION



ADC MODULE
VRH & VRL SELECTION



ADC MODULE
ANALOG SIGNAL FILTERS



BYPASS CAPACITORS, CLEAN POWER & SIGNAL FILTERS

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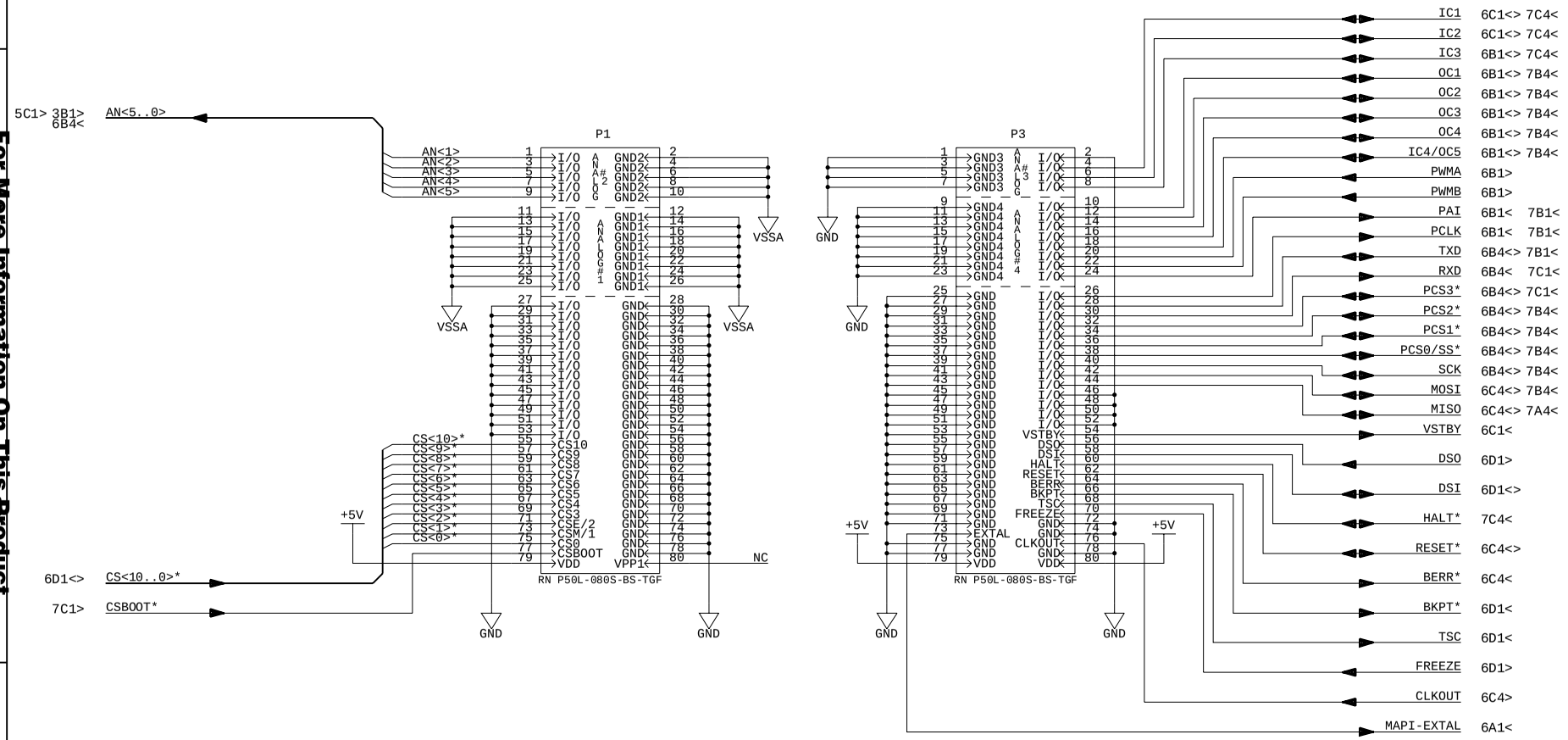
MAPI BUS P1

MAPI BUS P3



MODULAR ACTIVE PROBE INTERCONNECT P1 & P3

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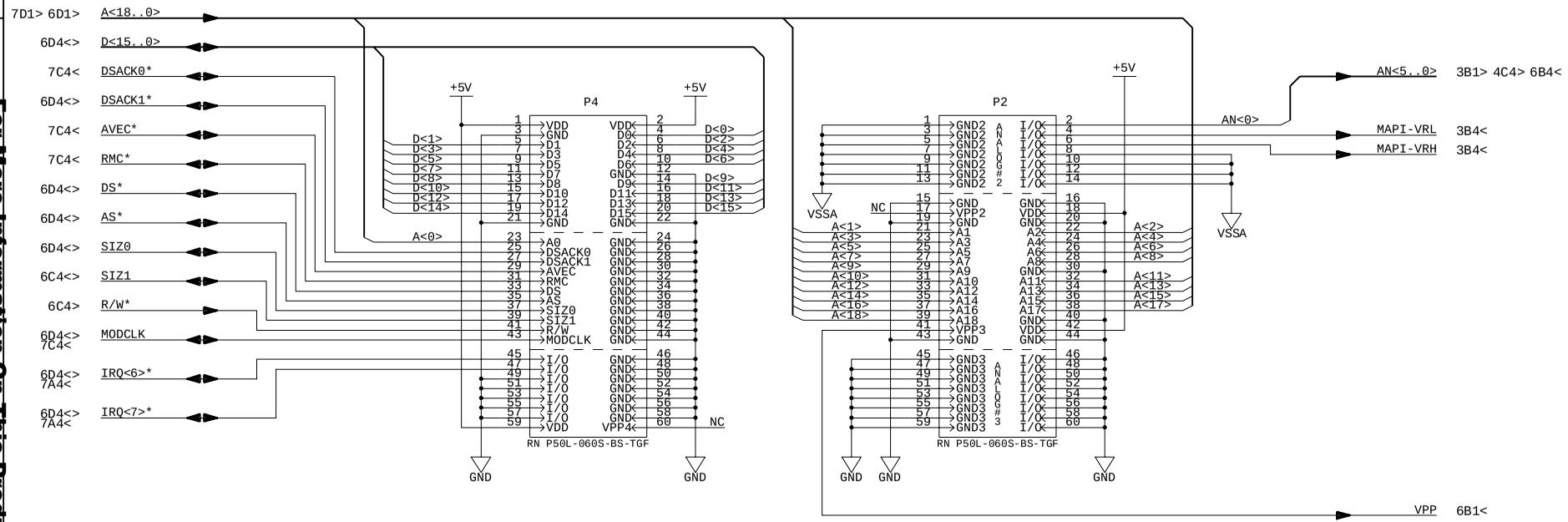

MODULAR ACTIVE PROBE INTERCONNECT P2 & P4

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63ASE90344W
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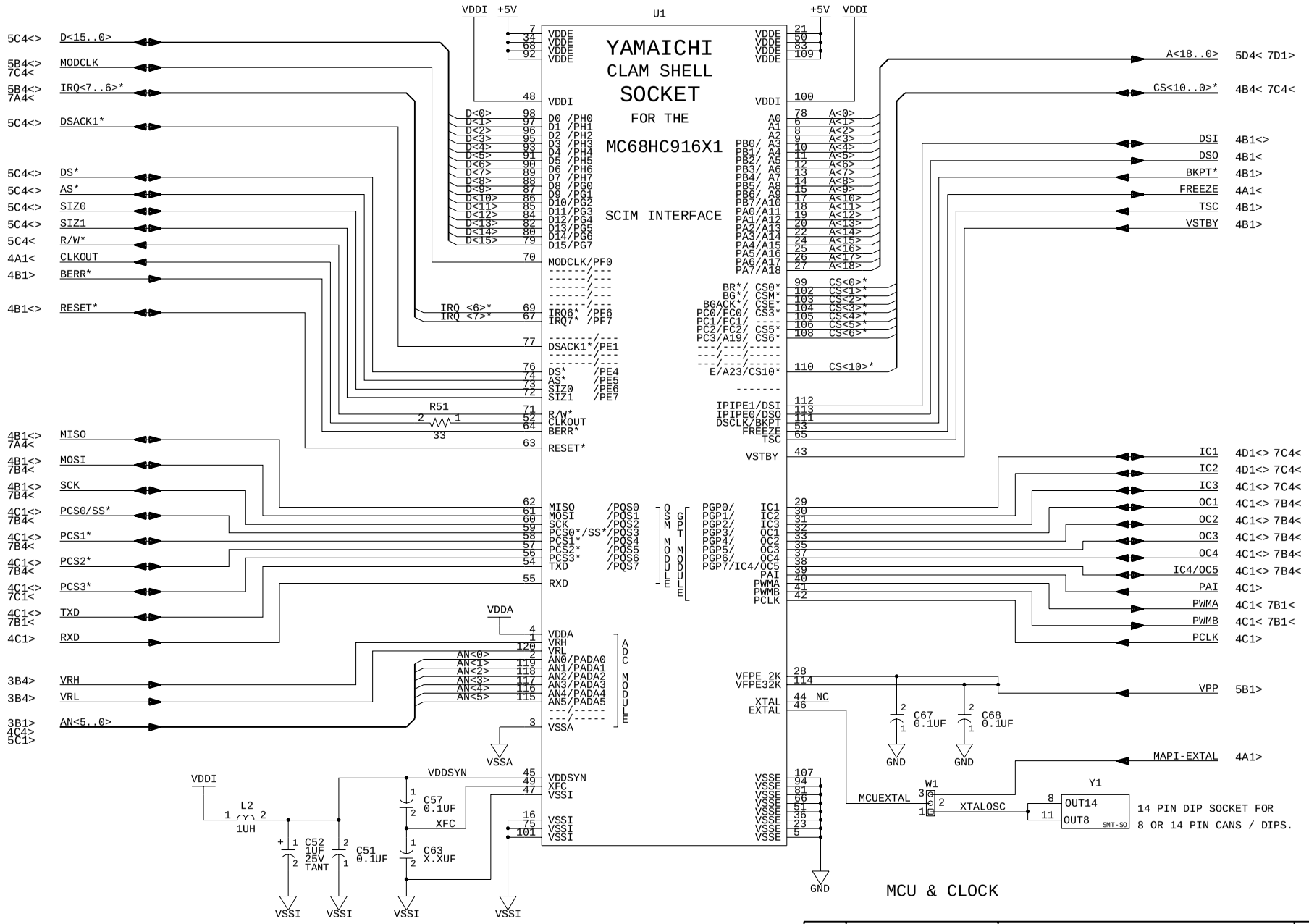

MCU & CLOCK

NOTE: 1) PLACE THE CAP BETWEEN VDDSYN & XFC AS CLOSE TO MCU PINS AS POSSIBLE.
2) THE CAP BETWEEN XFC & VSSI IS OPTIONAL.

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REV: A

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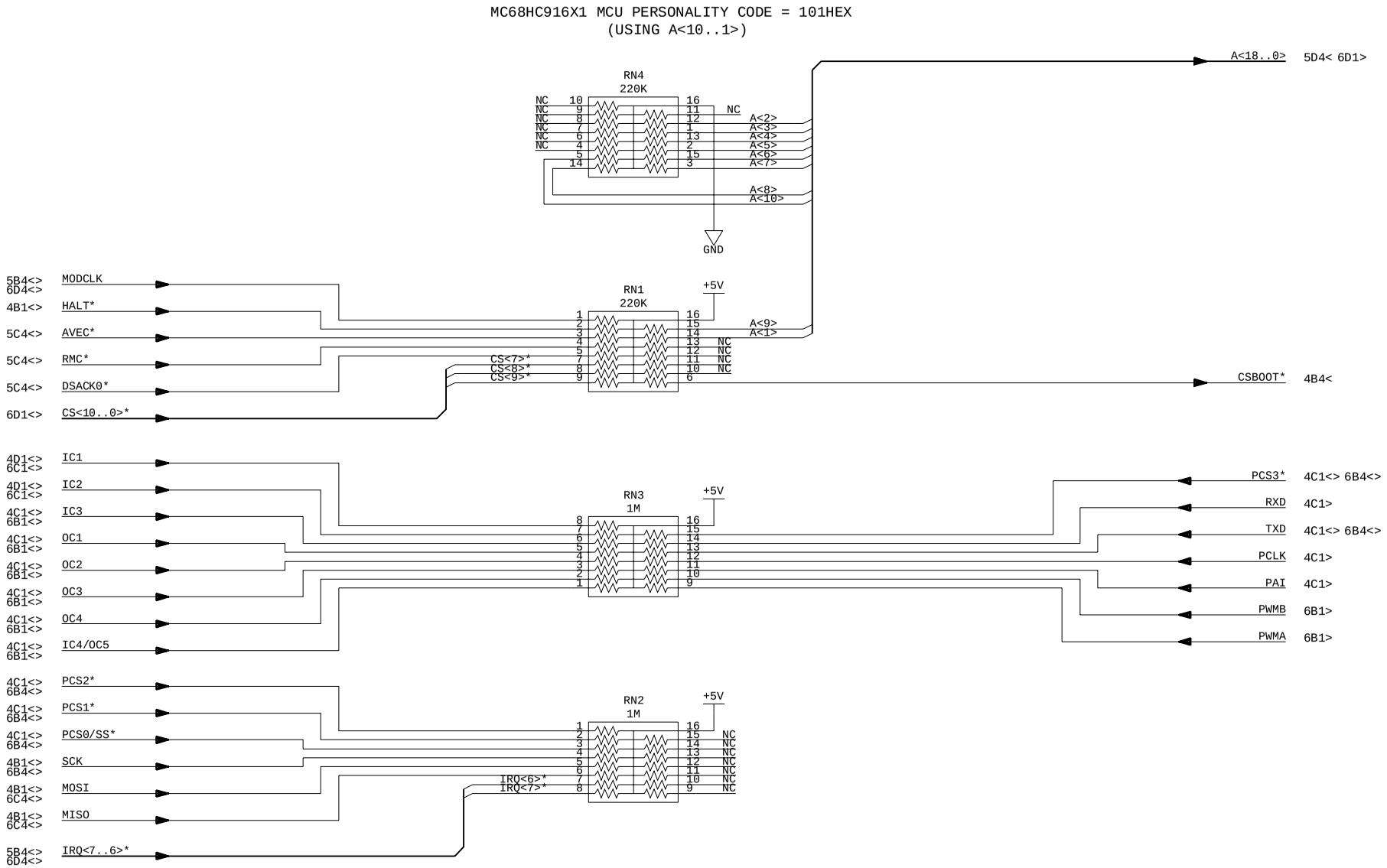

PULL-UPS / PULL-DOWNS / PERSONALITY ID

SIZE		DWG. NO.	REV:
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*** Signal Cross-Reference ***
--- for the entire design --

A <18..0>	5D4< 6D1> 7D1>
AN <5..0>	3B1> 4C4> 5C1> 6B4<
AS *	5C4<> 6D4<>
AVEC *	5C4<> 7C4<
BERR *	4B1> 6C4<
BKPT *	4B1> 6D1<
CLKOUT	4A1< 6C4>
CS <10..0> *	4B4< 6D1<> 7C4<
CSBOOT *	4B4< 7C1>
D <15..0>	5C4<> 6D4<>
DS *	5C4<> 6D4<>
DSACK0 *	5C4<> 7C4<
DSACK1 *	5C4<> 6D4<>
DSI	4B1<> 6D1<>
DSO	4B1< 6D1>
FREEZE	4A1< 6D1>
HALT *	4B1<> 7C4<
IC1	4D1<> 6C1<> 7C4<
IC2	4D1<> 6C1<> 7C4<
IC3	4C1<> 6B1<> 7C4<
IC4/OC5	4C1<> 6B1<> 7B4<
IRQ <7..6> *	5B4<> 6D4<> 7A4<
MAPI-EXTAL	4A1> 6A1<
MAPI-VRH	3B4< 5C1>
MAPI-VRL	3B4< 5C1>
MISO	4B1<> 6C4<> 7A4<
MODCLK	5B4<> 6D4<> 7C4<
MOSI	4B1<> 6C4<> 7B4<
OC1	4C1<> 6B1<> 7B4<
OC2	4C1<> 6B1<> 7B4<
OC3	4C1<> 6B1<> 7B4<
OC4	4C1<> 6B1<> 7B4<
PAI	4C1> 6B1< 7B1<
PCLK	4C1> 6B1< 7B1<
PCS0/SS *	4C1<> 6B4<> 7B4<
PCS1 *	4C1<> 6B4<> 7B4<
PCS2 *	4C1<> 6B4<> 7B4<
PCS3 *	4C1<> 6B4<> 7C1<
PWMA	4C1< 6B1> 7B1<
PWMB	4C1< 6B1> 7B1<
R/W *	5C4< 6C4>
RESET *	4B1<> 6C4<>
RMC *	5C4<> 7C4<
RXD	4C1> 6B4< 7C1<
SCK	4B1<> 6B4<> 7B4<
SIZ0	5C4<> 6D4<>
SIZ1	5C4<> 6C4<>
TSC	4B1> 6D1<
TXD	4C1<> 6B4<> 7B1<
VPP	5B1> 6B1<
VRH	3B4> 6B4<
VRL	3B4> 6B4<
VSTBY	4B1> 6C1<

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63ASE90344W REV: A

SIGNAL CROSS REFERENCES

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